Fig. 1

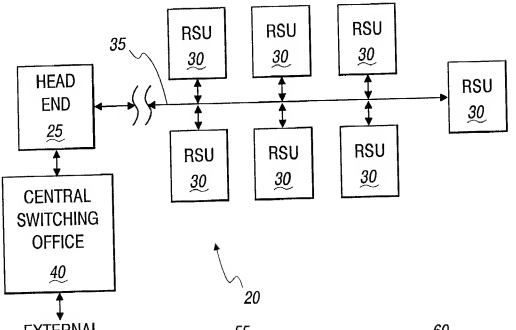

RSU
30
35
HEAD
END
25
CENTRAL
SWITCHING
OFFICE
40
EXTERNAL
20

Fig. 2

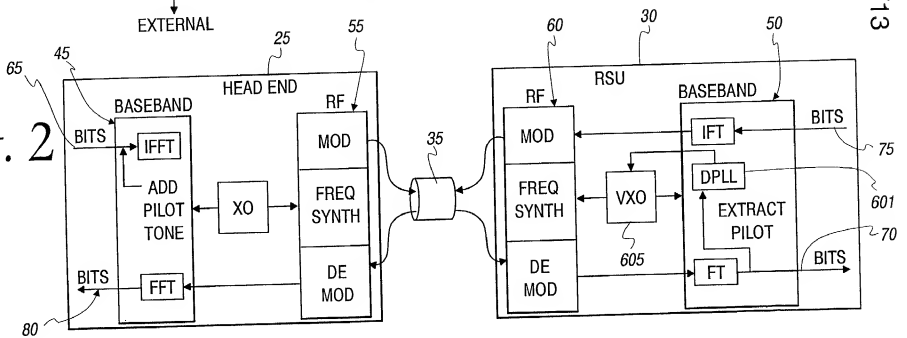
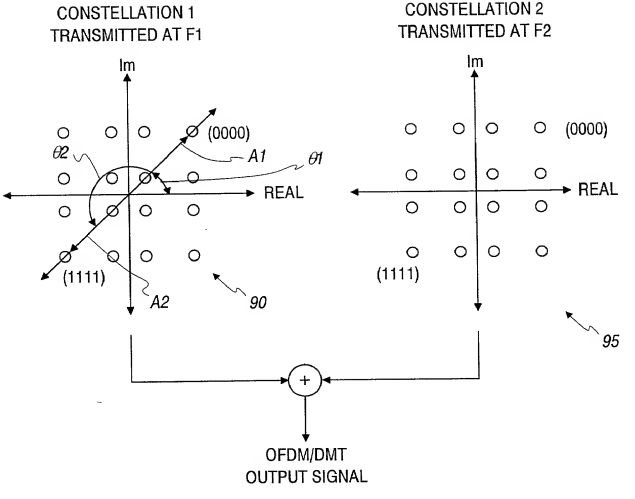

HEAD END
25
RSU
30
BASEBAND
RF
BITS
IFFT
ADD
PILOT
TONE
XO
MOD
FREQ
SYNTH
DE
MOD
FFT
35
45
55
60
50
65
75
601
70
605
80
IFT
DPLL
EXTRACT
PILOT
VXO
FT

Fig. 3


CONSTELLATION 1
TRANSMITTED AT F1
Im
(0000)
θ2
A1
θ1
REAL
(1111)
A2
90
CONSTELLATION 2
TRANSMITTED AT F2
Im
(0000)
REAL
(1111)
95
+
OFDM/DMT
OUTPUT SIGNAL

T05270 06621660

Fig. 4

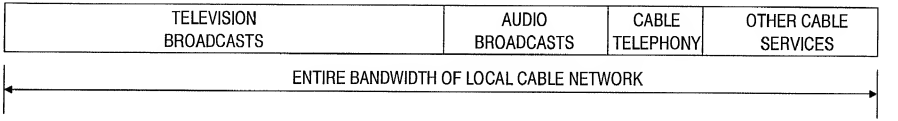


Fig. 6

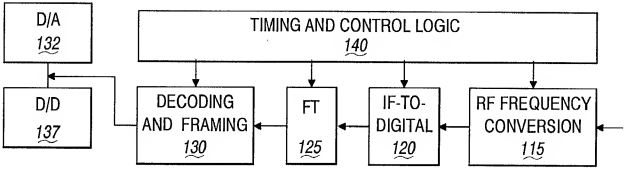


Fig. 5

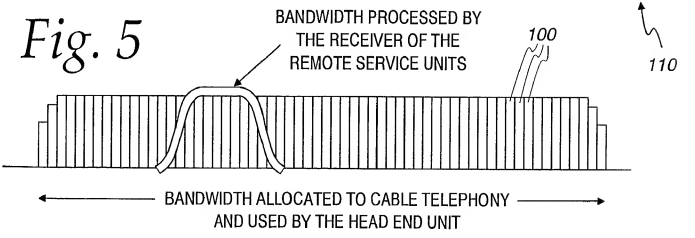


Fig. 7

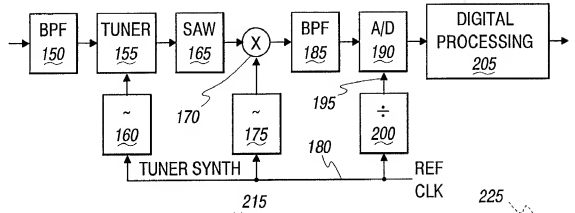

BPF 150
TUNER 155
SAW 165
X
BPF 185
A/D 190
DIGITAL PROCESSING 205
~ 160
170
~ 175
195
÷ 200
180
TUNER SYNTH
REF CLK

Fig. 8

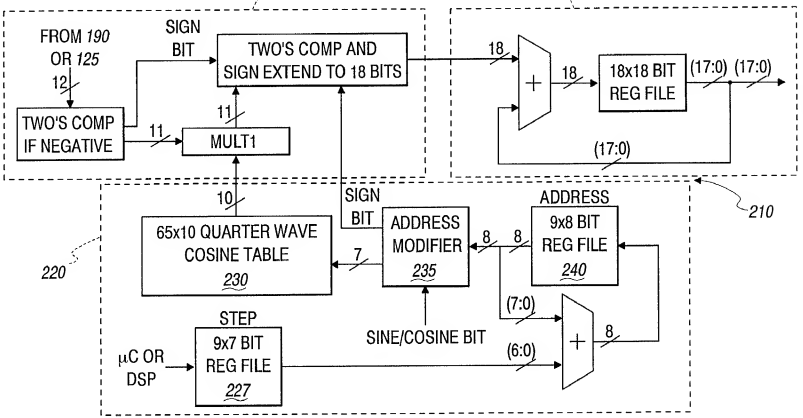

215
225
FROM 190 OR 125
12
SIGN BIT
TWO'S COMP AND SIGN EXTEND TO 18 BITS
18
18
18x18 BIT REG FILE
(17:0)
(17:0)
TWO'S COMP IF NEGATIVE
11
11
MULT1
(17:0)
210
10
SIGN BIT
ADDRESS
65x10 QUARTER WAVE COSINE TABLE 230
ADDRESS MODIFIER 235
8
8
9x8 BIT REG FILE 240
7
220
(7:0)
STEP
SINE/COSINE BIT
8
µC OR DSP
9x7 BIT REG FILE 227
(6:0)

Fig. 9

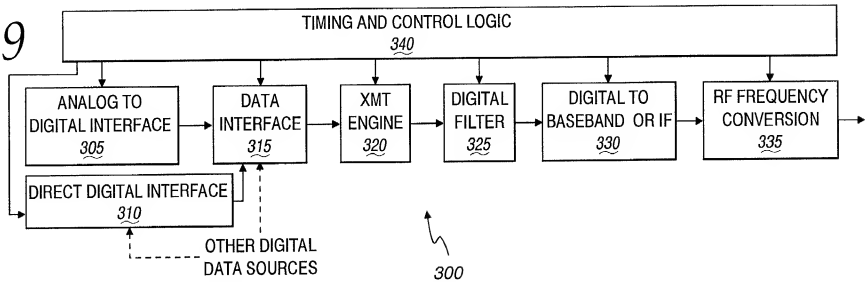
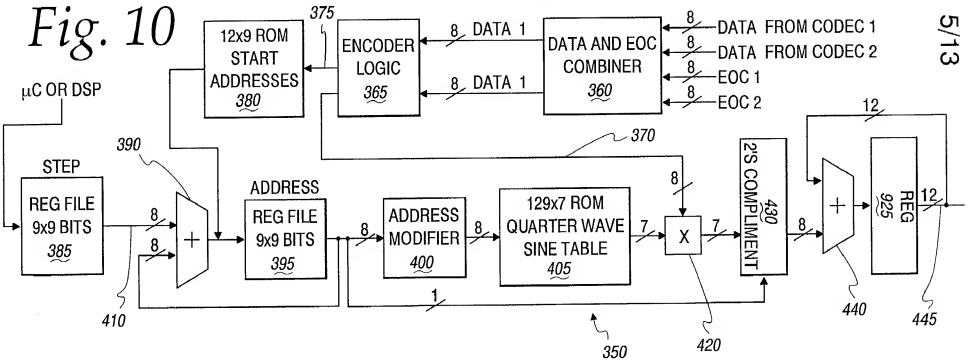

TIMING AND CONTROL LOGIC
340
ANALOG TO DIGITAL INTERFACE
305
DATA INTERFACE
315
XMT ENGINE
320
DIGITAL FILTER
325
DIGITAL TO BASEBAND OR IF
330
RF FREQUENCY CONVERSION
335
DIRECT DIGITAL INTERFACE
310
OTHER DIGITAL DATA SOURCES
300

Fig. 10


µC OR DSP
STEP
REG FILE 9x9 BITS
385
390
410
ADDRESS
REG FILE 9x9 BITS
395
12x9 ROM START ADDRESSES
380
375
ENCODER LOGIC
365
8 DATA 1
8 DATA 1
DATA AND EOC COMBINER
360
8 DATA FROM CODEC 1
8 DATA FROM CODEC 2
8 EOC 1
8 EOC 2
370
ADDRESS MODIFIER
400
129x7 ROM QUARTER WAVE SINE TABLE
405
X
2'S COMPLIMENT
430
REG
925
12
440
445
350
420

FOSS20 0662T650

Fig. 11

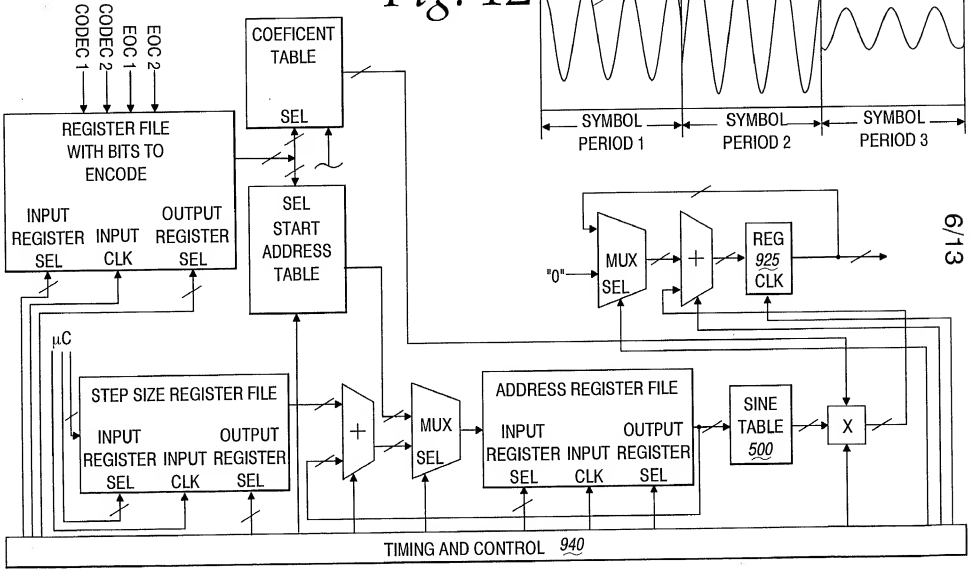
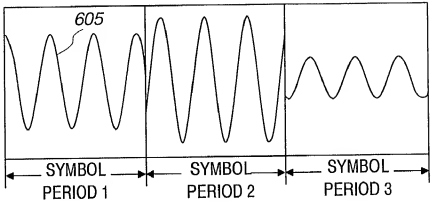


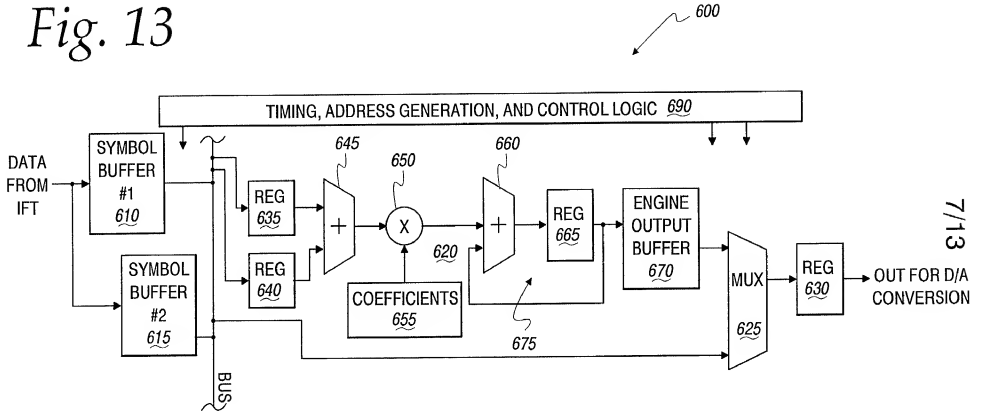
Fig. 12



6/13

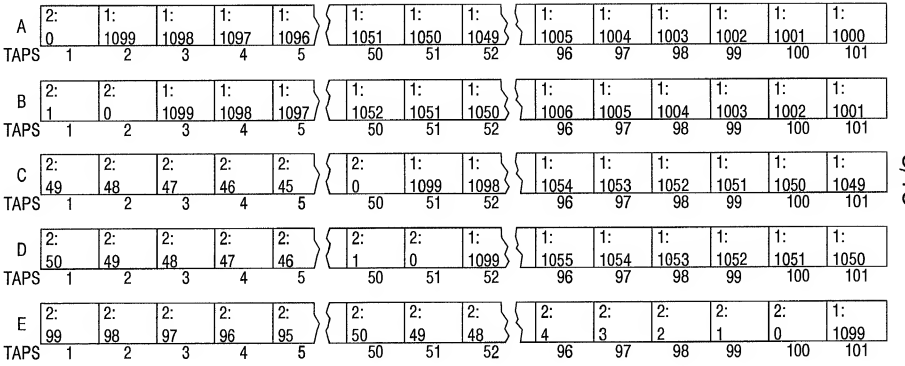
09912990 .070501

Fig. 13



0991299O .0725O4

Fig. 14



TOSZ0:0562T660

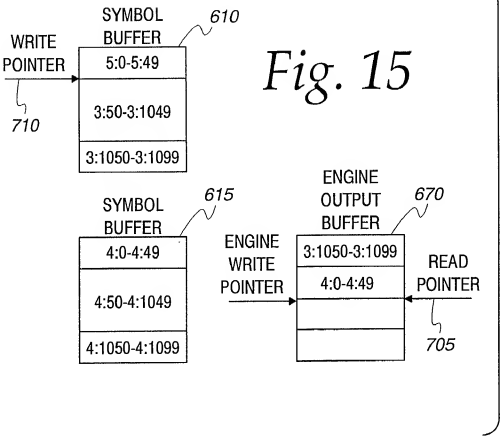


Fig. 15

Fig. 16

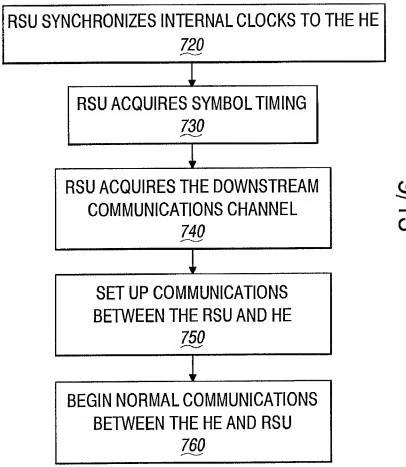
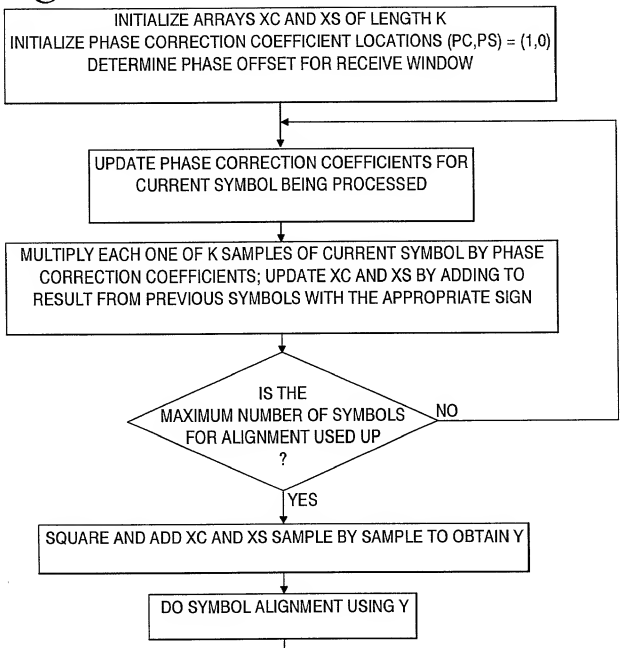


Fig. 16B



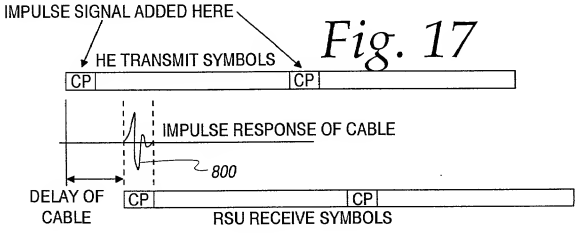


Fig. 17

Fig. 18

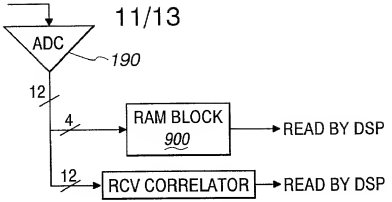


Fig. 19

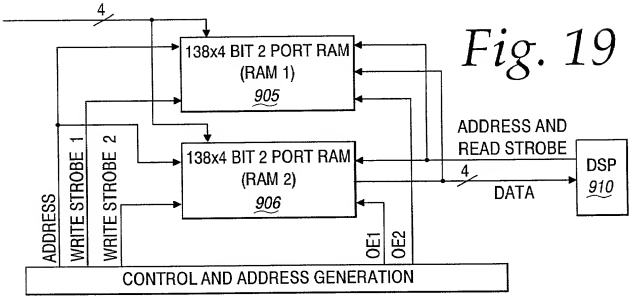


Fig. 20

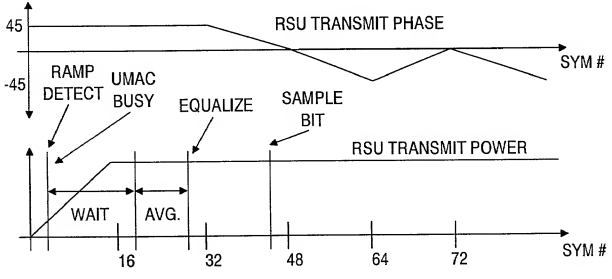


Fig. 21

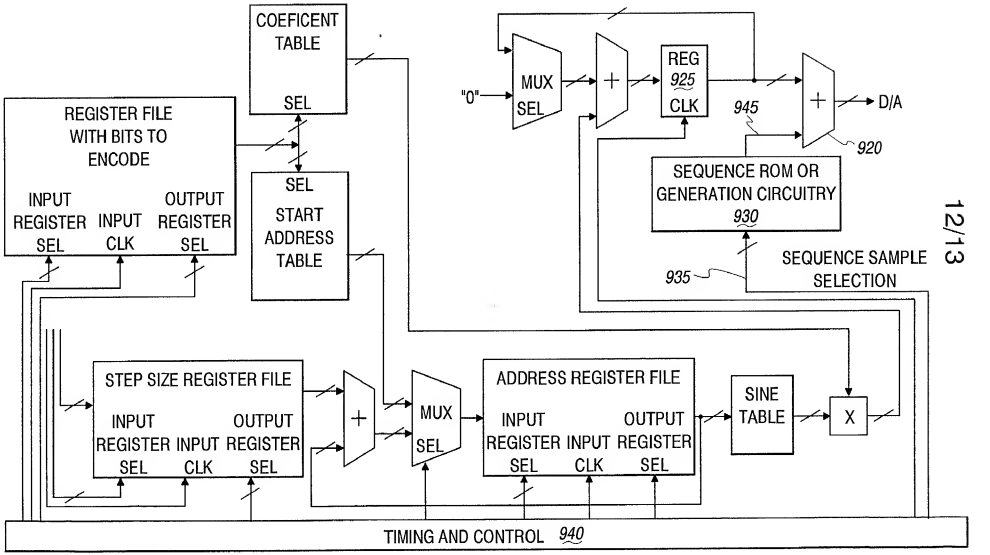
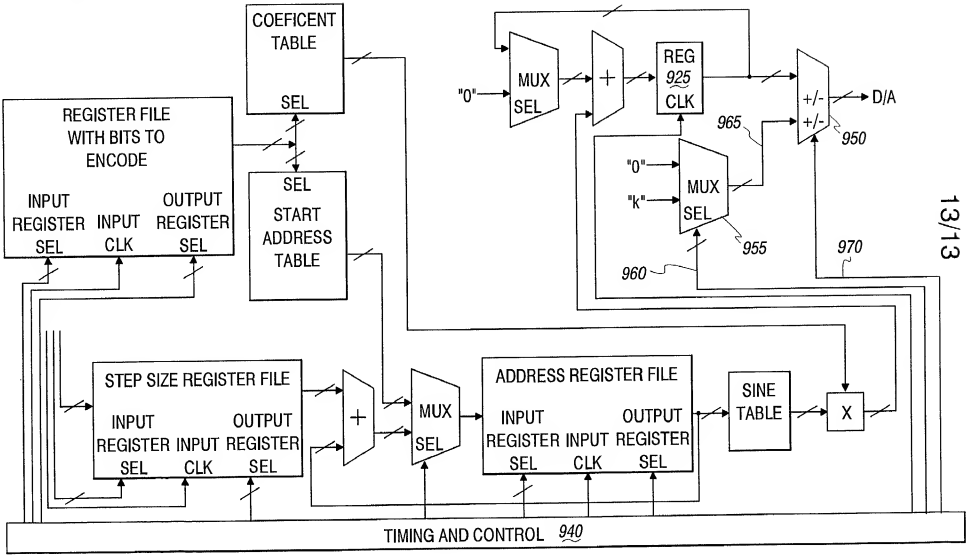

COEFICENT TABLE
SEL
REGISTER FILE WITH BITS TO ENCODE
INPUT REGISTER SEL
INPUT CLK
OUTPUT REGISTER SEL
SEL
START ADDRESS TABLE
"0"
MUX
SEL
+
REG
925
CLK
945
+
D/A
920
SEQUENCE ROM OR GENERATION CIRCUITRY
930
SEQUENCE SAMPLE SELECTION
935
STEP SIZE REGISTER FILE
INPUT REGISTER SEL
INPUT CLK
OUTPUT REGISTER SEL
+
MUX
SEL
ADDRESS REGISTER FILE
INPUT REGISTER SEL
INPUT CLK
OUTPUT REGISTER SEL
SINE TABLE
X
TIMING AND CONTROL 940

Fig. 22


COEFICENT TABLE
SEL
REGISTER FILE WITH BITS TO ENCODE
INPUT REGISTER SEL
INPUT CLK
OUTPUT REGISTER SEL
SEL
START ADDRESS TABLE
"0"
MUX SEL
+
REG 925 CLK
+/-
+/-
D/A
965
950
"0"
"k"
MUX SEL
955
960
970
STEP SIZE REGISTER FILE
INPUT REGISTER SEL
INPUT CLK
OUTPUT REGISTER SEL
+
MUX SEL
ADDRESS REGISTER FILE
INPUT REGISTER SEL
INPUT CLK
OUTPUT REGISTER SEL
SINE TABLE
X
TIMING AND CONTROL 940